GLONASS – Single Difference Phase Biases

Scope of study

GLONASS observations experience various hardware delays for each transmitting satellite (or each frequency) named "inter-channel biases". The frequency-specific hardware biases complicate resolution of double-difference phase ambiguity. Studies in the past showed that phase biases depend on the used receiver and antenna, whose design improve all the time and it is worthwhile to repeat respective studies. A data set from 6 state-of-the-art receivers from 3 different manufactures have been connected to a single antenna and tracked GPS and GLONASS satellites. The zero-baseline test scenario holds the important advantage to know the "ground truth" of ambiguities (double difference ambiguity are „zero" from geometry).

Tracking Scenario

GLONASS Observable

Double Difference Phase Observable

$$\Phi_{kl}^{ij} = c \cdot \Phi_{kl}^{ij} + N_{kl}^{ij} \cdot \lambda^i - N_{kl}^{ij} \cdot \lambda^{ij} + c \cdot t_{kl(ij)}$$

Single Difference Bias $\quad N_{kl}^i \cdot \lambda^{ij}$

Inter-Channel Bias $\quad c \cdot t_{kl(ij)} + \underbrace{c \cdot (t_{k(i)} - t_{k(j)})}_{a} + \underbrace{c \cdot (t_{l(i)} - t_{l(j)})}_{b}$

Case I: Receiver clock error is equal for all satellites (freq.)
$a = b = 0$, no inter-channel bias.

Case II: Inter-channel bias is equal for receivers k and l
$a = b \neq 0$, no inter-channel bias.

Case III: Inter-channel biases is different for receivers k and l
$a \neq b$, inter-channel bias present.
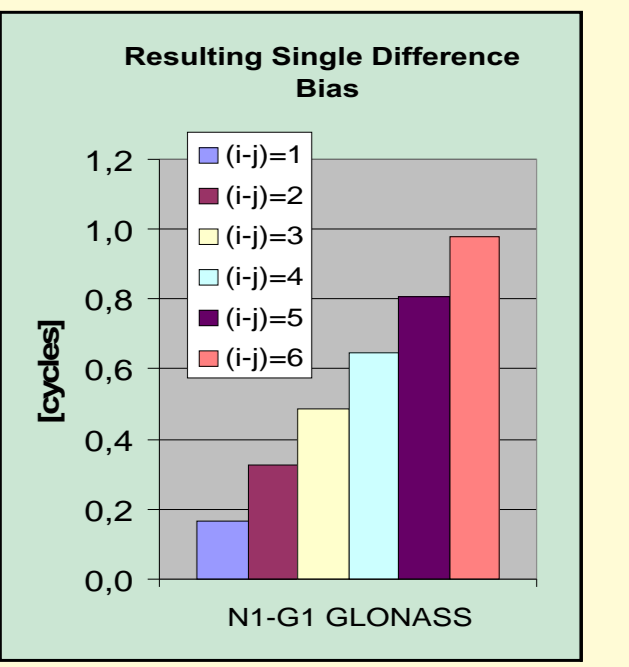
GLONASS Stand-Alone Approach

Even the successful combination of GPS and GLONASS nowadays obviously will not improve the resulting co-ordinates compared to GPS stand-alone processing. This behavior may be explained by the fact that the formal error of a GLONASS stand-alone solution is significant larger than for a GPS stand-alone one. Thus the formal error of the combination of both will be larger than the GPS stand-alone approach. This is the motivation to intensively study the GLONASS stand-alone processing approach. The observation data for this study have been tracked in November 2007 and 13 GLONASS satellites have been operational during that time.

Receiver Clock Difference

Results and Conclusion

The receiver clock difference will provoke a frequency dependent single-difference bias term in double-difference phase ambiguities, because of inaccurate single-difference ambiguity initialization. The magnitude of this bias has been predicted from the estimated receiver clocks and validated from GLONASS, L1 phase analysis. As soon as the receiver clocks have been considered in the calculation of a-priori single-difference ambiguities, the double-difference ambiguity result clearly to be integer. We conclude that phase data of modern receiver types don't suffer from any inter-channel bias.
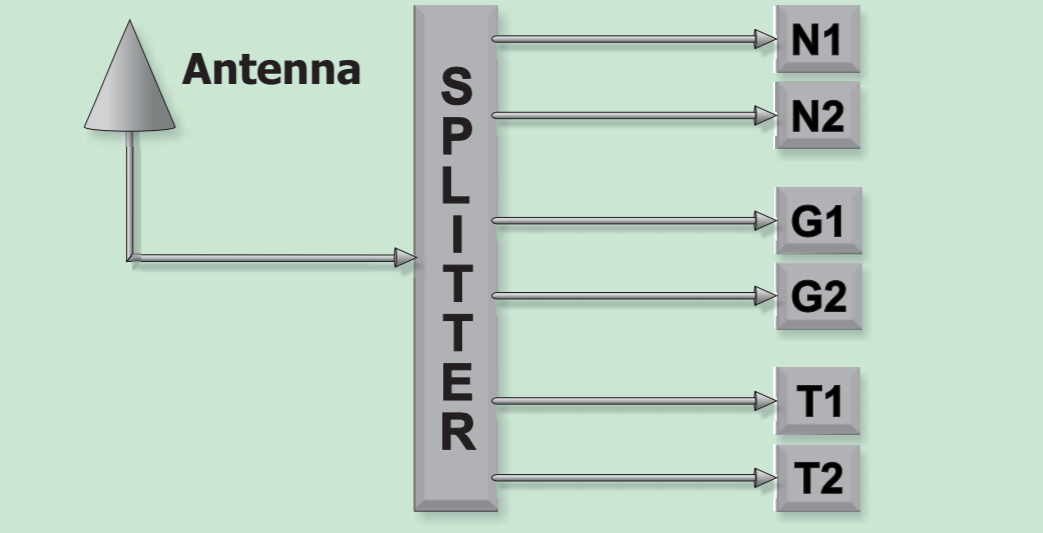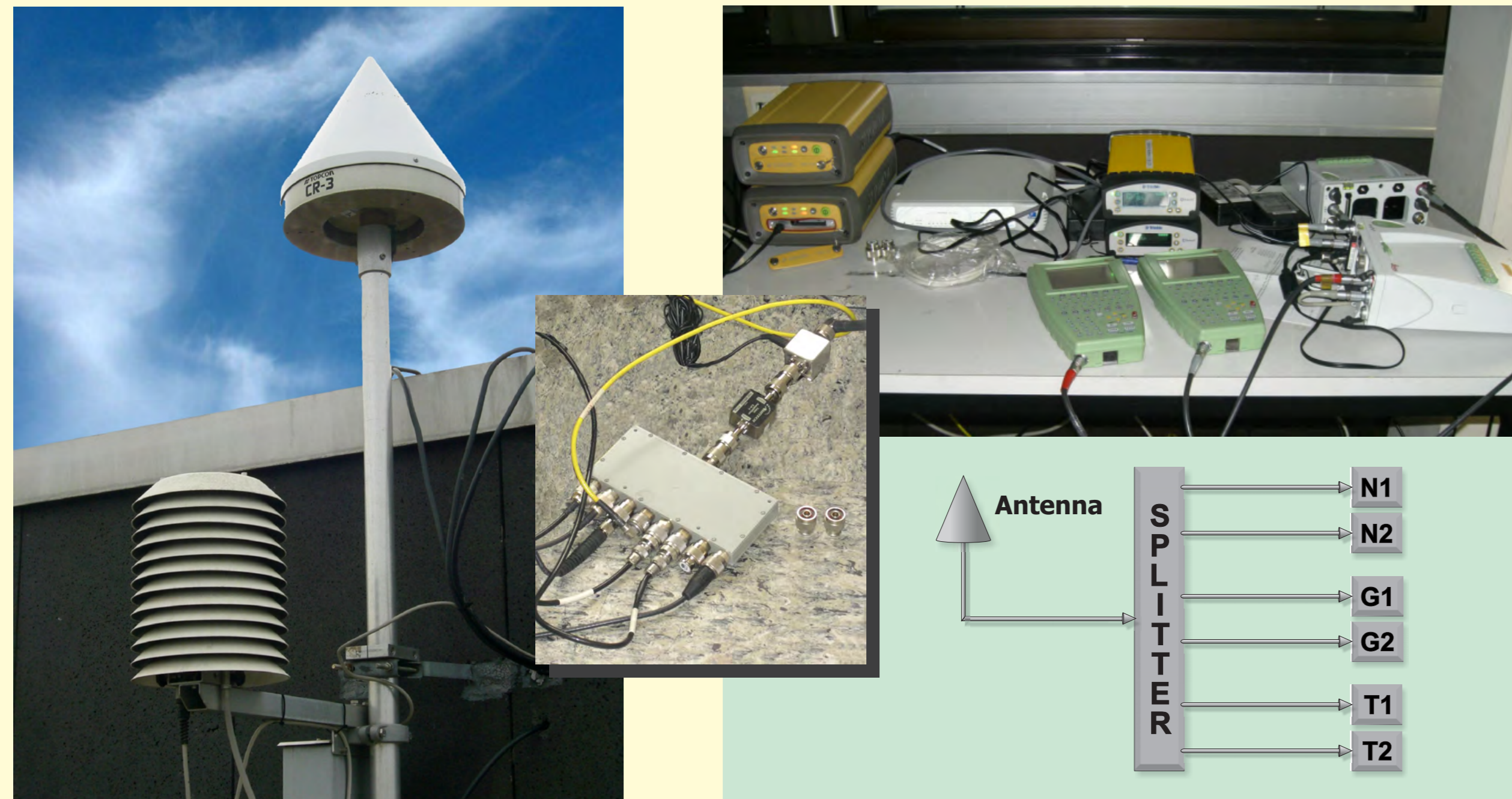
Resulting Ambiguity (1)

Biased estimates

DD-ambiguities are formed from real estimates of SD-ambiguities and grouped by color according to frequency differences. The plot on the right shows the mean of each group.

Slot No.	Freq. No.	Init. Amb.	Estimated SD-Amb.
115	0	0	1,55
106	1	0	1,72
124	2	0	1,88
123	3	0	2,04
110	4	0	-1,8
110	4	0	-1,8
107	5	0	1,36
108	6	0	1,53
108	6	0	-14489112,47

SD-Amb.	1,55	1,72	1,88	2,04	-1,8	-1,8	1,36	1,53	-14489112,47
1,55	0	0,17	0,33	0,49	0,65	0,65	0,81	0,98	0,979999999
1,72	0,17	0	0,16	0,32	0,48	0,48	0,64	0,81	0,809999999
1,88	0,33	0,16	0	0,16	0,32	0,32	0,48	0,65	0,649999999
2,04	0,49	0,32	0,16	0	0,16	0,16	0,32	0,49	0,49
-1,8	-3,35	-3,52	-3,68	-3,84	0	0,16	0,33	0,33
-1,8	-3,35	-3,52	-3,68	-3,84		0	0,16	0,33	0,33
1,36	-0,19	-0,36	-0,52	-0,68	3,16	3,16	0	0,17	0,17
1,53	-0,02	-0,19	-0,35	-0,51	3,33	3,33	0,17	0	0
-14489112,47	-14489114,02	-14489114,19	-14489114,35	-14489114,51	-14489110,67	-14489110,67	-14489113,83	-14489114	
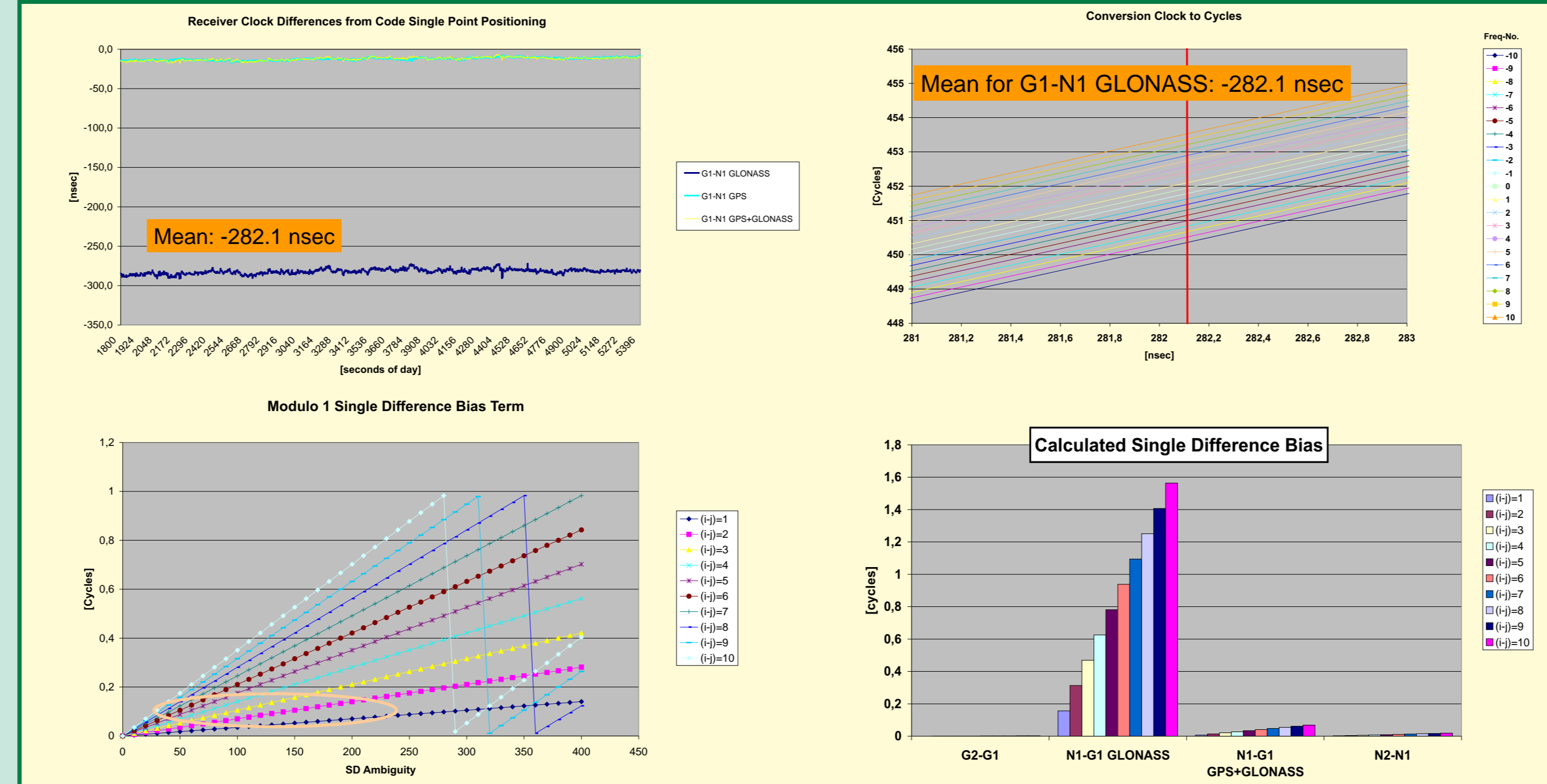
Resulting Ambiguity (2)

Constraining one DD ambiguity

This solution overcomes the problem of incorrect initialization of the single difference ambiguities by constraining one double difference ambiguity to "zero". The introduction of this constraint becomes possible, because of the situation of the zero baseline. Estimated SD ambiguities correspond to the SD receiver clock.

Slot No.	Freq. No.	Init. Amb.	Estimated SD-Amb.
115	0	0	-453,87
106	1	0	-453,87
124	2	0	fixed
123	3	0	-453,86
110	4	0	-457,86
110	4	0	-457,86
107	5	0	-454,86
108	6	0	-454,86
108	6	0	-1448968,86

SD-Amb.	-453,87	-453,87	fixed	-453,86	-457,86	-457,86	-454,86	-454,86	-1448968,86
-453,87	0	0		0,01	0,01	0,01	0,01	0,01	0,01
-453,87	0	0		0,01	0,01	0,01	0,01	0,01	0,01
fixed									
-453,86	0,01	0,01		0	0	0	0	0	0
-457,86	-3,99	-3,99		-4	0	0	0	0	0
-457,86	-3,99	-3,99		-4	0	0	0	0	0
-454,86	-0,99	-0,99		-1	3	3	0	0	0
-454,86	-0,99	-0,99		-1	3	3	0	0	0
-1448968,86	-1448514,99	-1448514,99		-1448515	-1448511	-1448511	-1448514	-1448514	0

Resulting Ambiguity (3)

Consideration of SD-receiver clock in ambiguity initialization

Slot No.	Freq. No.	Init. Amb.	Estimated SD-Amb.
115	0	-456	-455,12
106	1	-456	-455,11
124	2	-456	-455,11
123	3	-456	-455,11
110	4	-458	-459,11
110	4	-458	-459,11
107	5	-457	-456,11
108	6	-457	-456,10
108	6	-14489567	-14489570,10

Index-Diff i-j
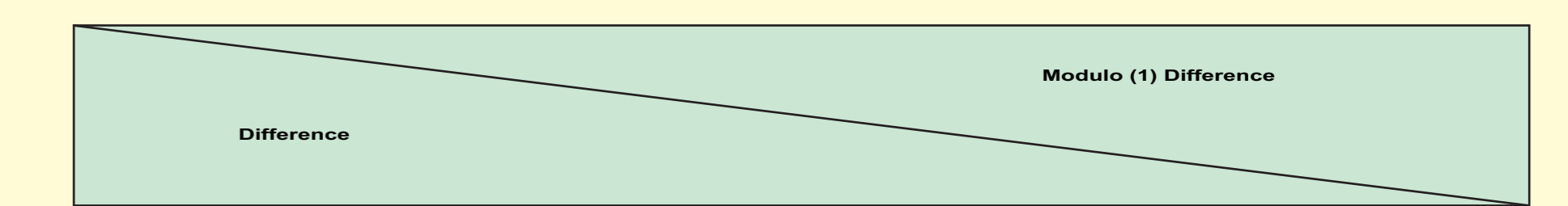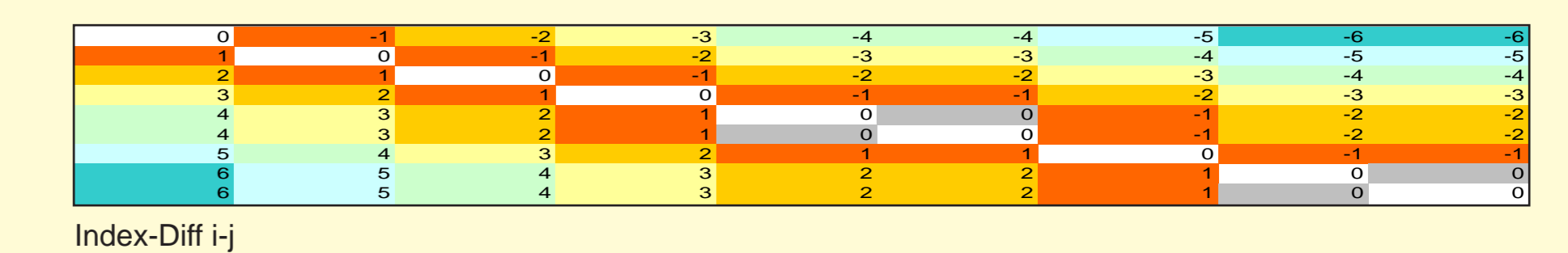
SD-Amb.	-455,12	-455,11	-455,11	-455,11	-459,11	-459,11	-456,11	-456,1	-14489570,1
-455,12	0	0,01	0,01	0,01	0,01	0,01	0,01	0,02	0,02
-455,11	0,01	0	0	0	0	0	0	0,01	0,01
-455,11	0,01	0	0	0	0	0	0	0,01	0,01
-455,11	0,01	0	0	0	0	0	0	0,01	0,01
-459,11	-3,99	-4	-4	-4	0	0	0	0,01	0,01
-459,11	-3,99	-4	-4	-4		0	0	0,01	0,01
-456,11	-0,99	-1	-1	-1	3	3	0	0,01	0,01
-456,1	-0,98	-0,99	-0,99	-0,99	3,01	3,01	0,01	0	0
-14489570,1	-14489114,98	-14489114,99	-14489114,99	-14489114,99	-14489110,99	-14489110,99	-14489113,99	-14489114	

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IGS Workshop 2008